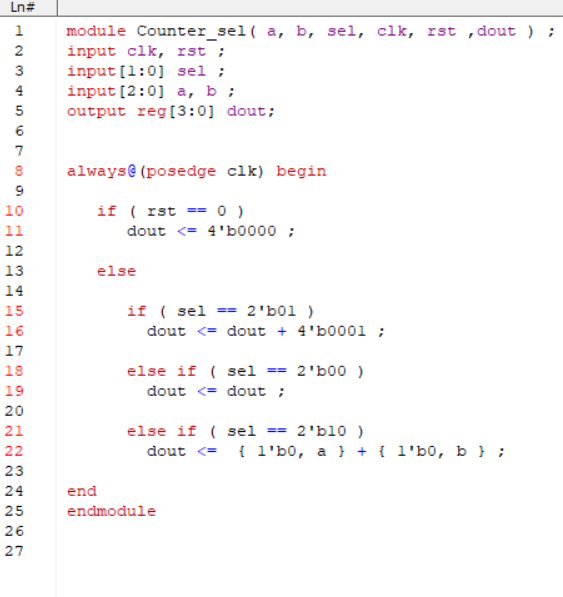
**Verilog Lab測驗**

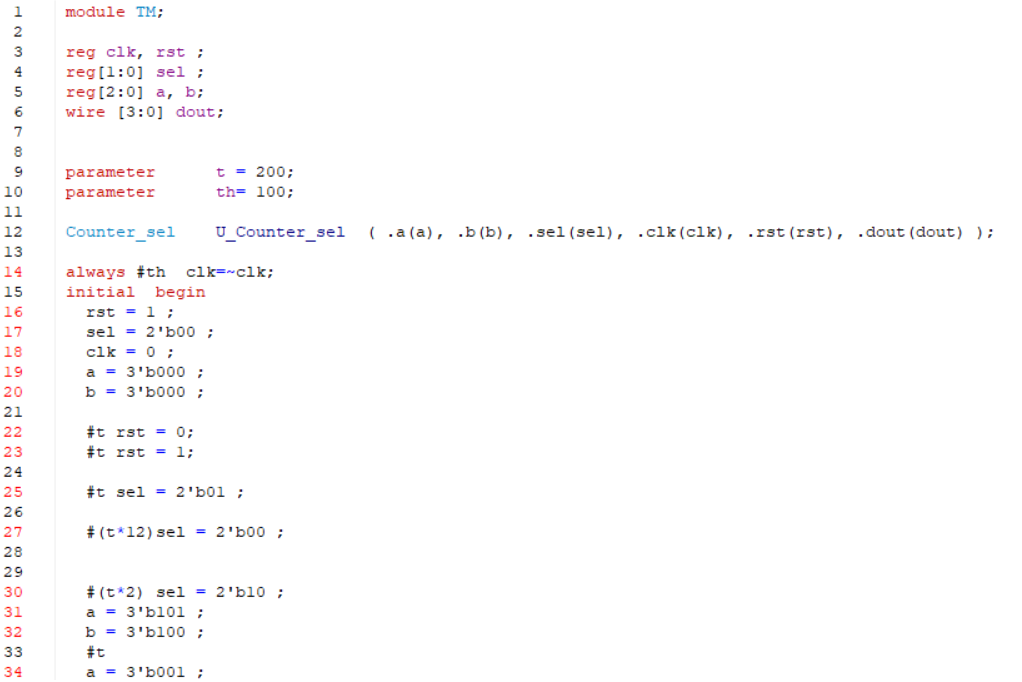
班級: 資工二乙

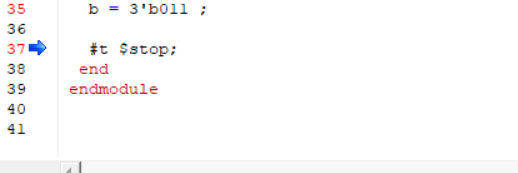
姓名: 蒲品憶

學號: 10927207

Counter



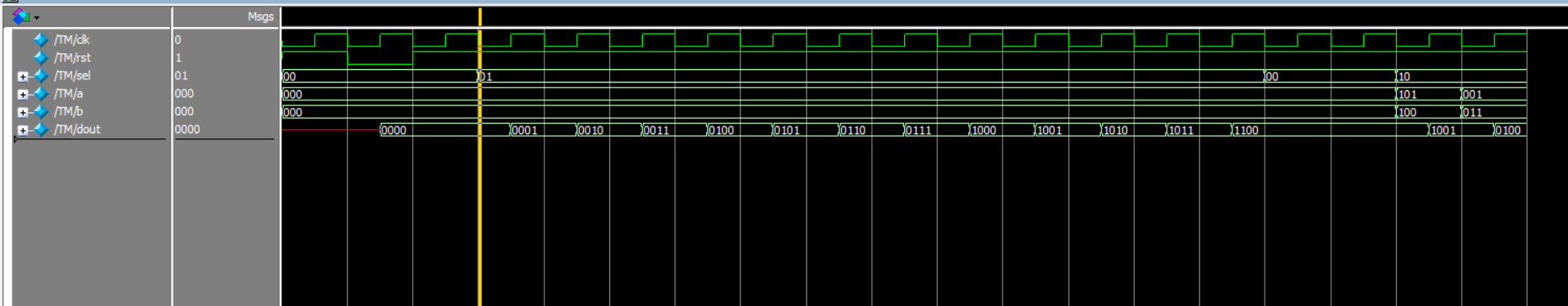
TM



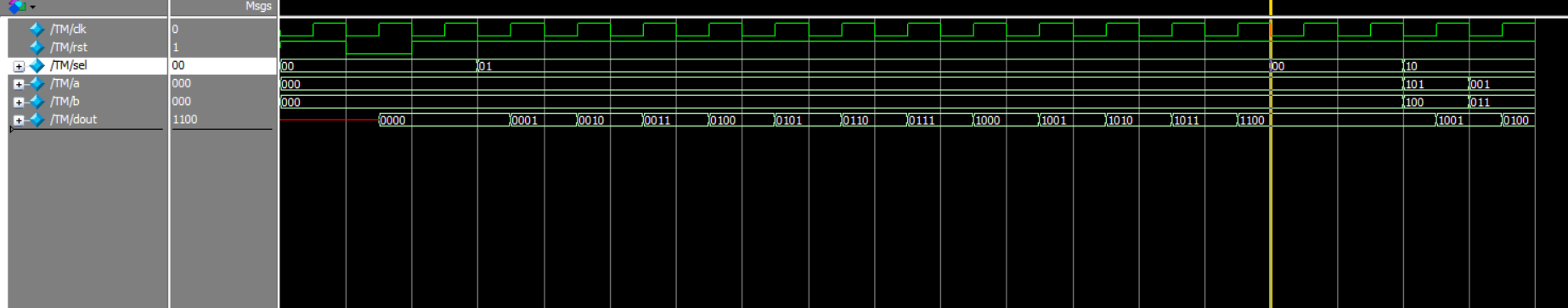
Wave

當rst = 0 時 dout = 0

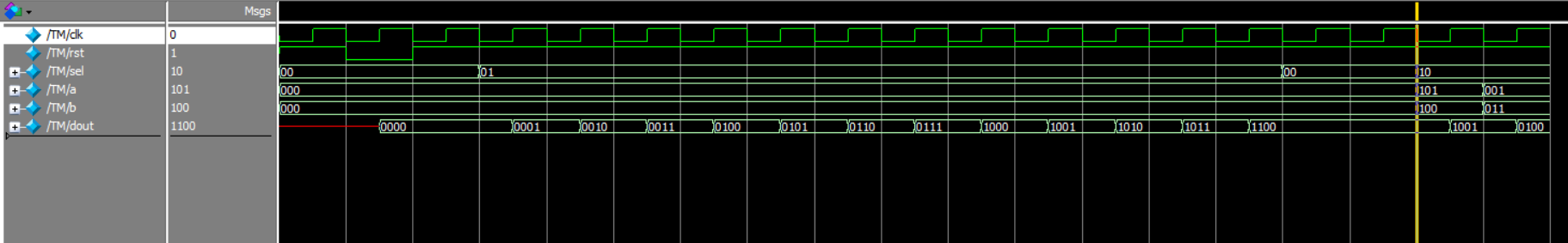
當rst = 1 時



sel = 01 , dout = dout + 1



sel = 00 , dout = dout



sel = 10, dout = { 1’b0, a } + { 1’b0,. b }

pwd

